Predictable implementation of avionics applications on MPPA

Journée thématique Verimag : Many-core Kalray MPPA, implementation and verification

April 29th 2019

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return on innovation

Outline

- ❑ Quentin Perret – Cifre PhD (2014 – 2017)
- ❑ CAPACITES / Collaboration (2015 – 2019)
- ❑ ONERA Internal Project – MACSIMA (2014 – 2018)
- ❑ Conclusion – future works

Temporal Isolation of Hard Real-Time Applications on Many-core Processors

Airbus Cifre PhD (2014 – 2017): Quentin Perret

Supervisors: Pascal Maurère, Eric Noulard, Claire Pagetti, Pascal Sainrat, Benoit Triquet

Quentin Perret, Pascal Maurère, Eric Noulard, Claire Pagetti, Pascal Sainrat, Benoit Triquet: Temporal Isolation of Hard Real-Time Applications on Many-Core Processors. RTAS 2016: 37-47

Quentin Perret, Pascal Maurère, Éric Noulard, Claire Pagetti, Pascal Sainrat, Benoît Triquet: Mapping hard real-time applications on many-core processors. RTNS 2016: 235-244

Quentin Perret, Pascal Maurère, Éric Noulard, Claire Pagetti, Pascal Sainrat, Benoît Triquet. Predictable composition of memory accesses on many-core processors. In Embedded Real Time Software ERTS 2016.

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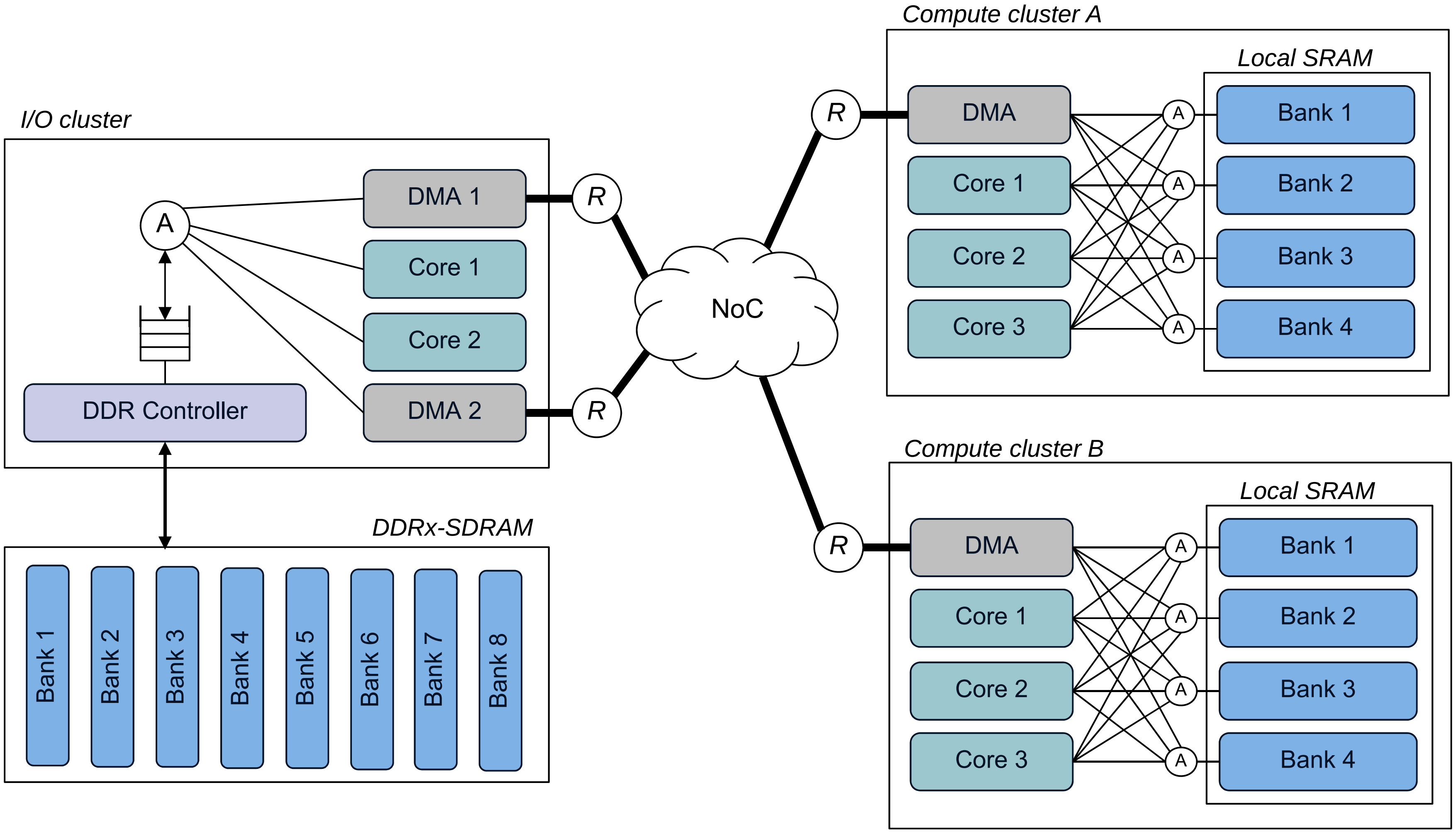
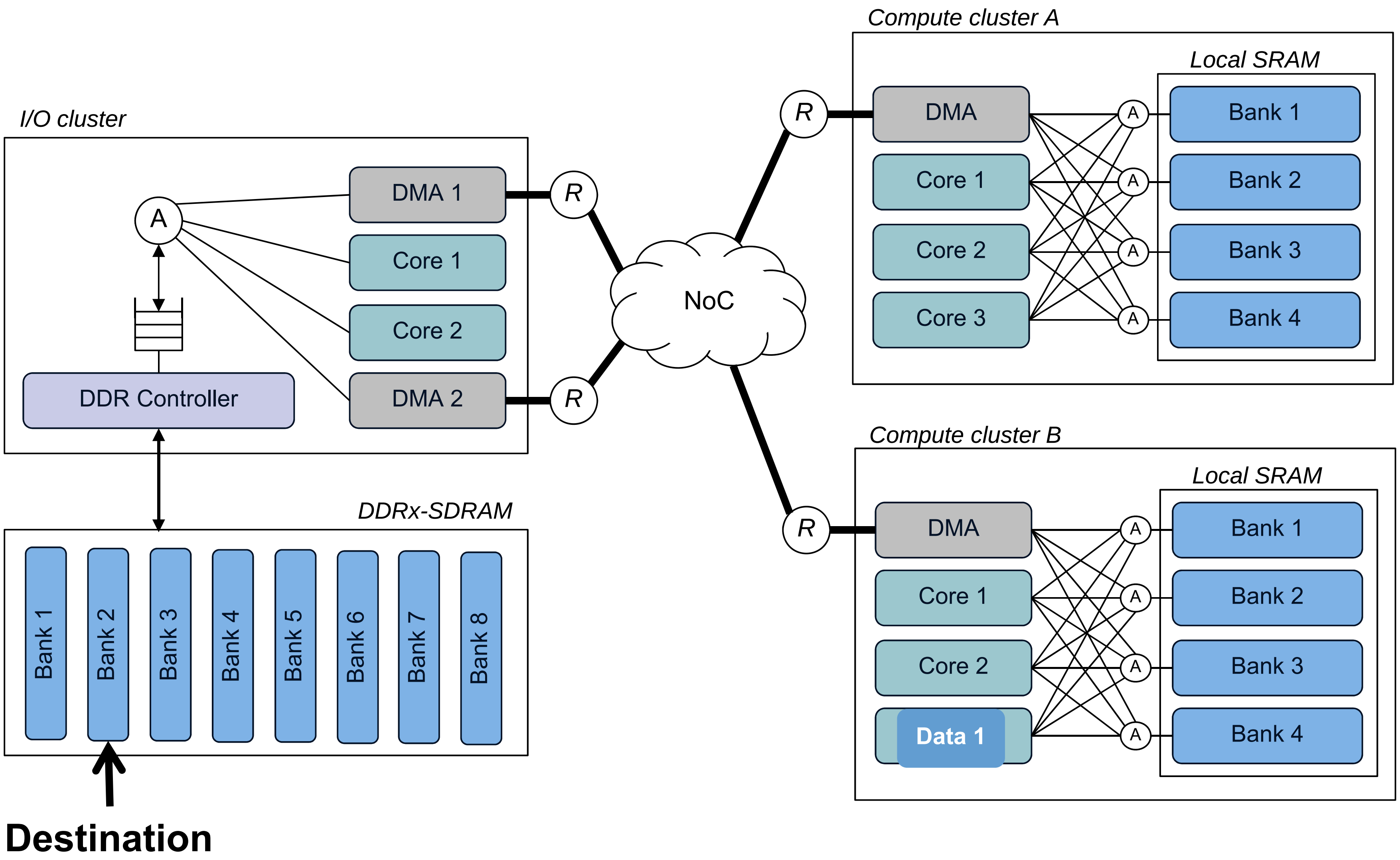
Example Kalray: accesses to the external memory



Example Kalray: accesses to the external memory



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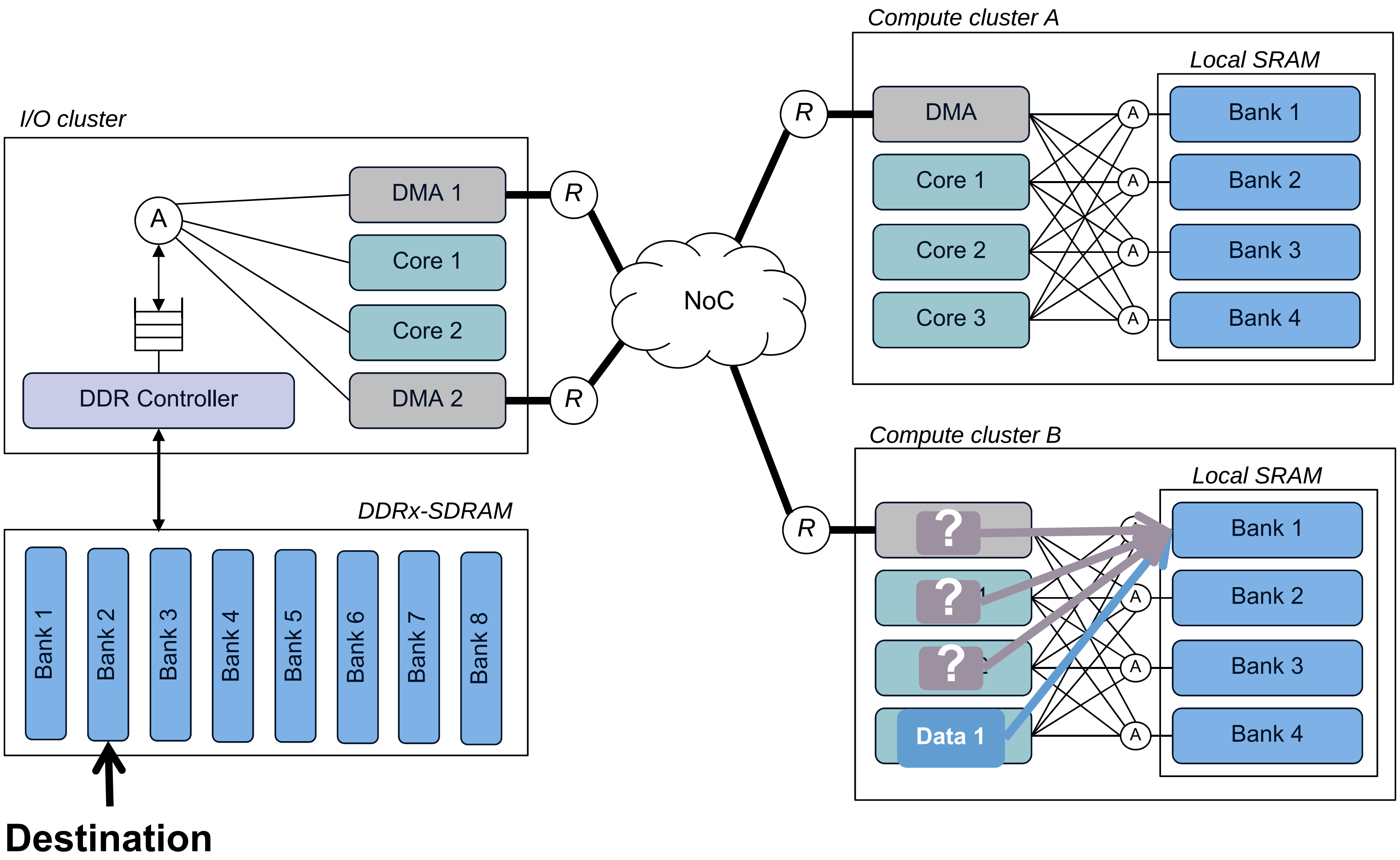

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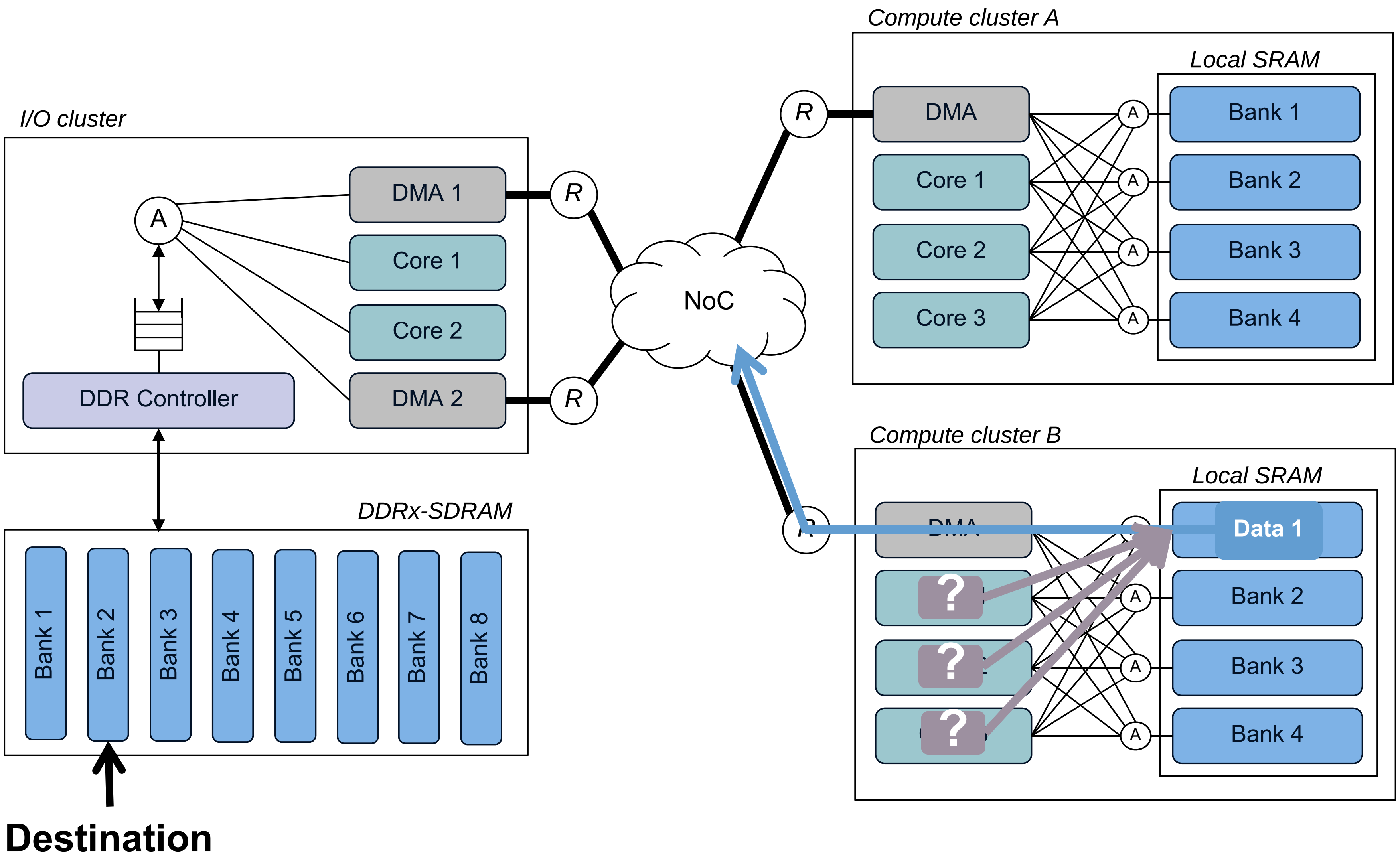

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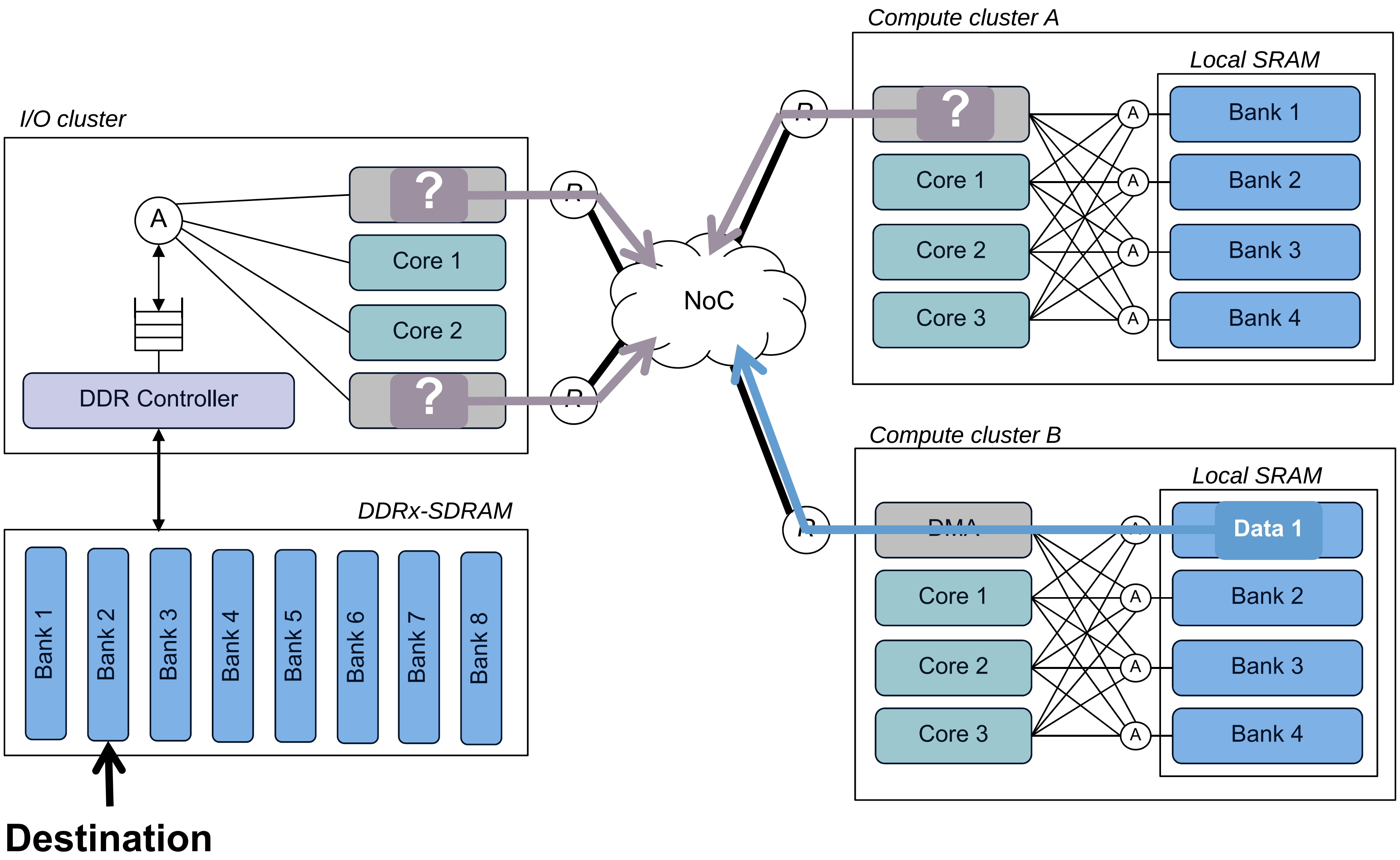
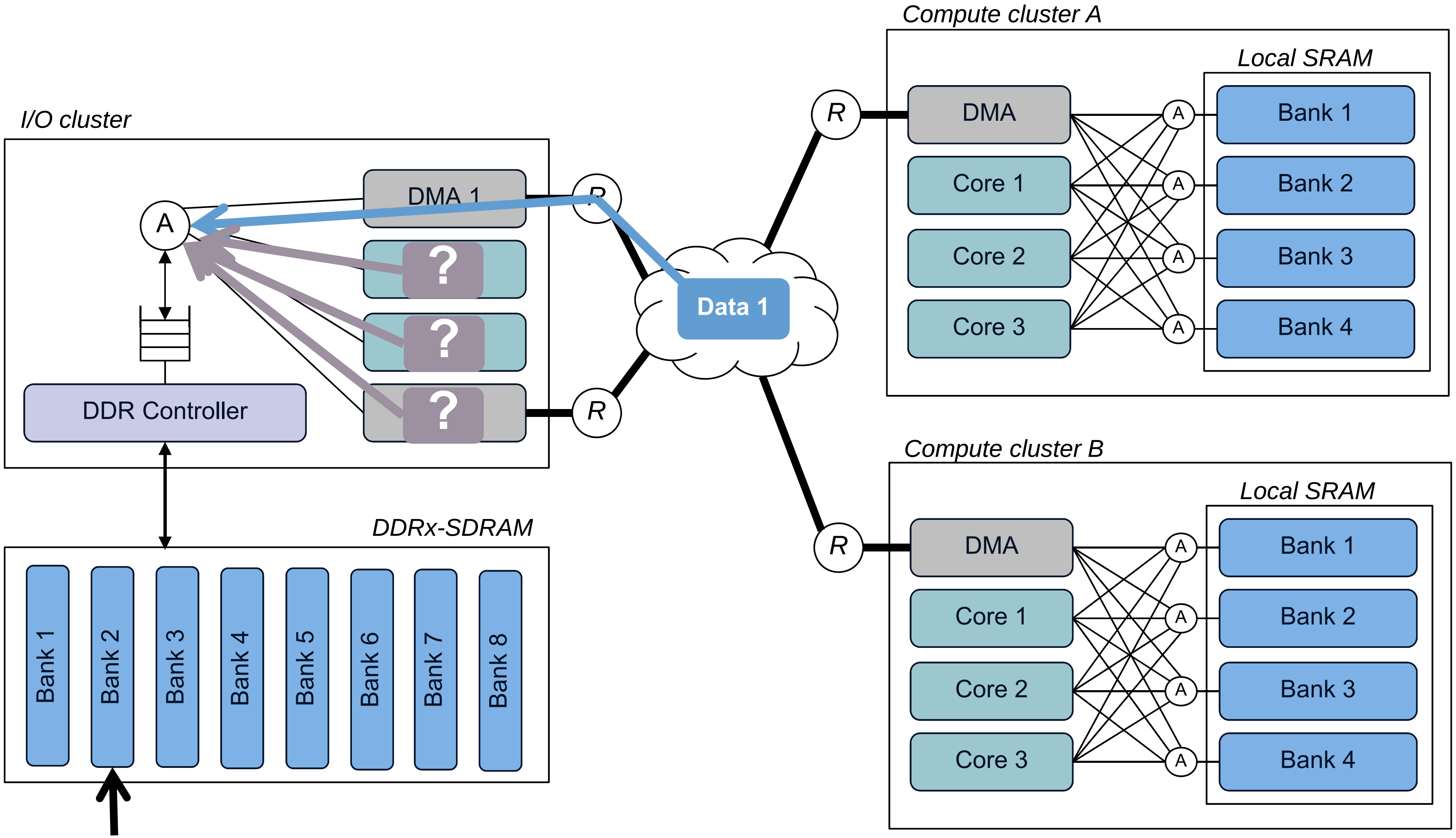
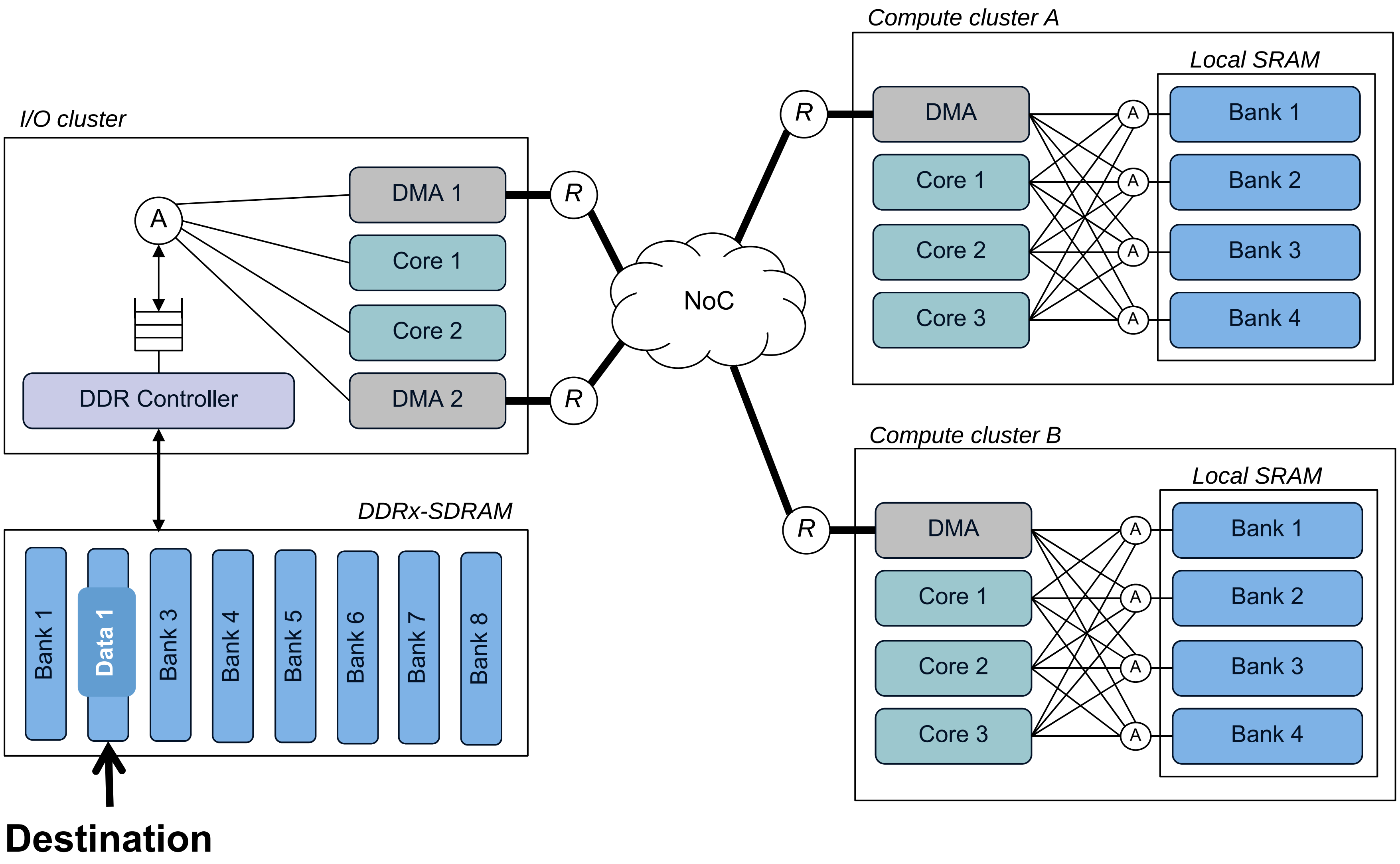


Example Kalray: accesses to the external memory



Destination

Example Kalray: accesses to the external memory



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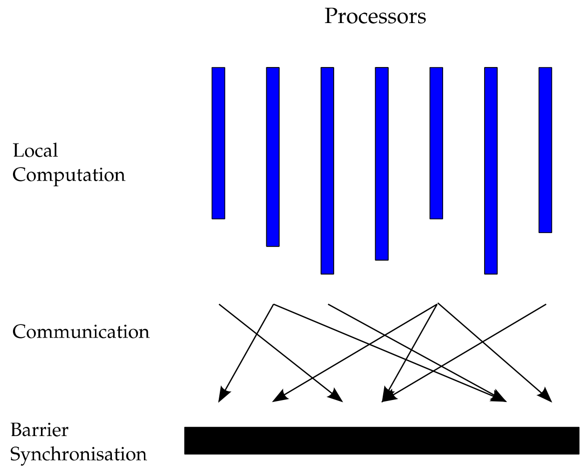
Execution models

- **Definition: set of rules to be followed by the designer in order to avoid or at least reduce the non predictable behaviours**

- **Origin: performance prediction models:**

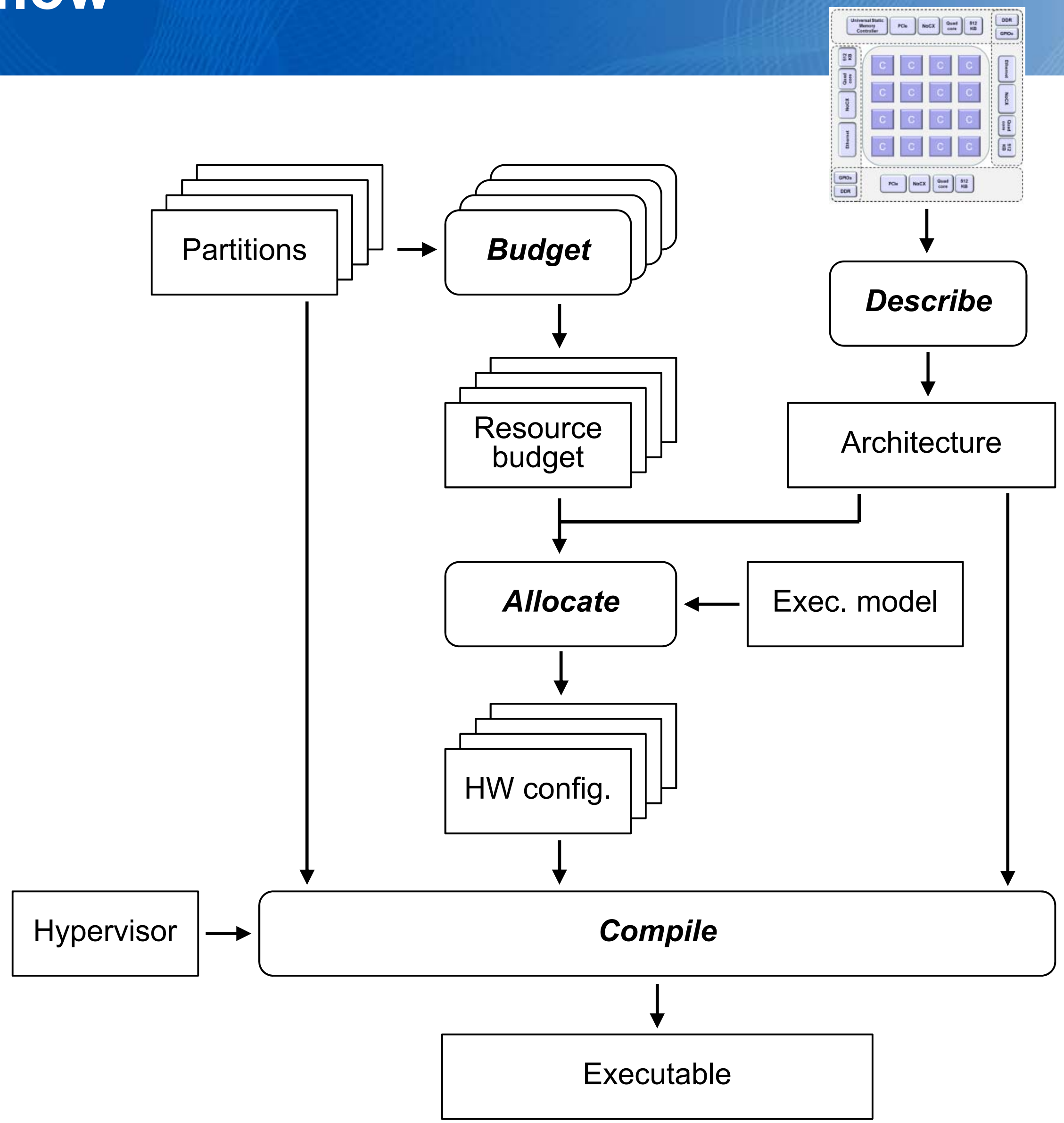
  Bulk synchronous parallel model



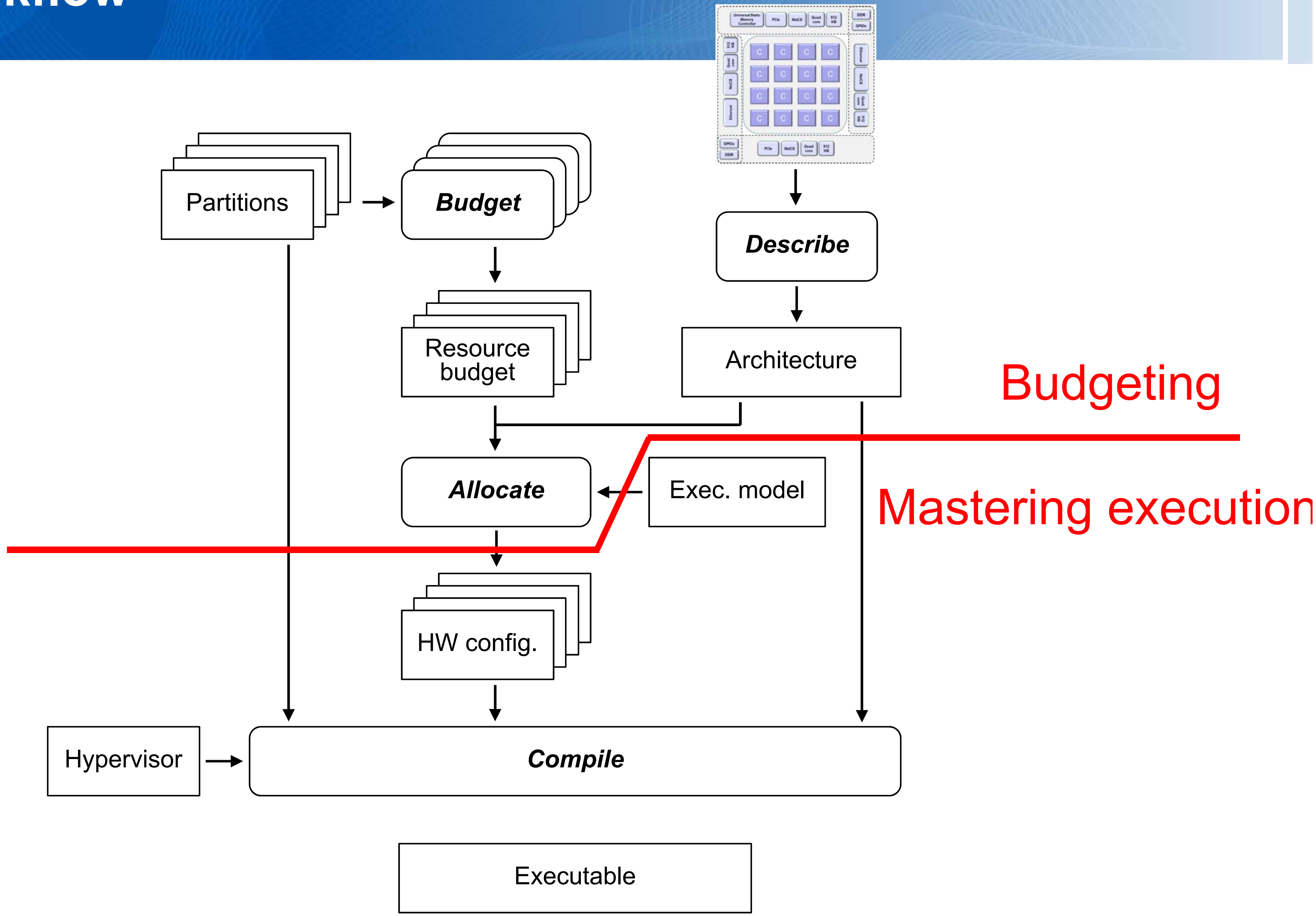
- **Principle: enforce and segregate the accesses to the shared resources to master them**

Works realised within several industrial projects (Airbus, Thales), a PhD with Airbus, internal projects (SCC) and regional project (2 post-doc TOAST/TORRENTS)

Workflow


Partitions
Budget
Describe
Resource budget
Architecture
Allocate
Exec. model
HW config.
Hypervisor
Compile
Executable

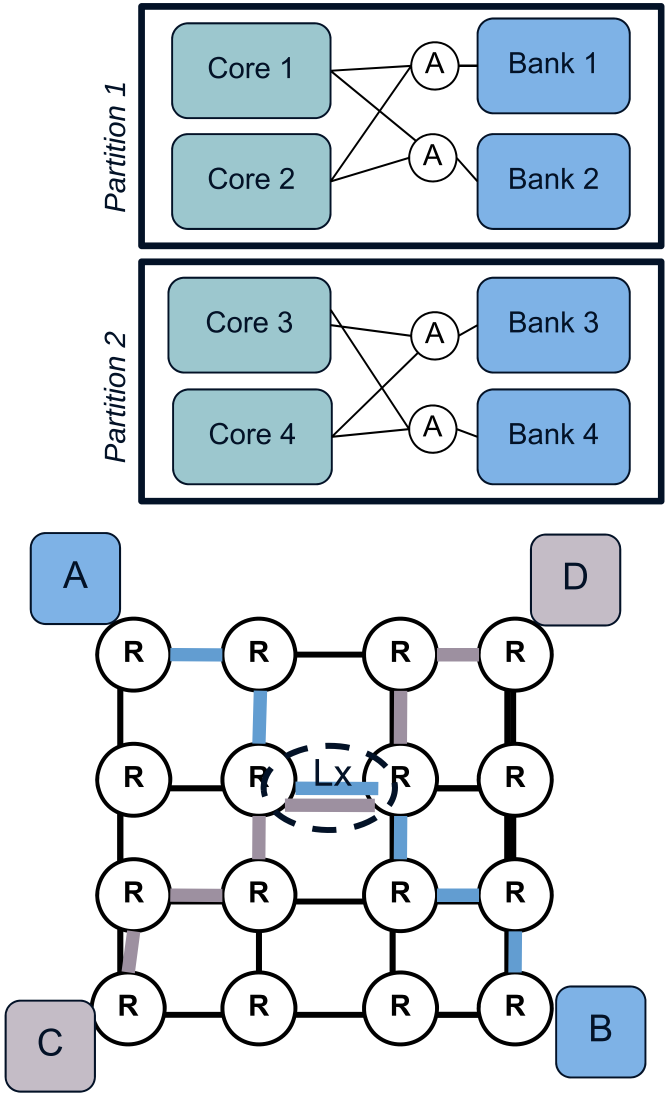
Workflow



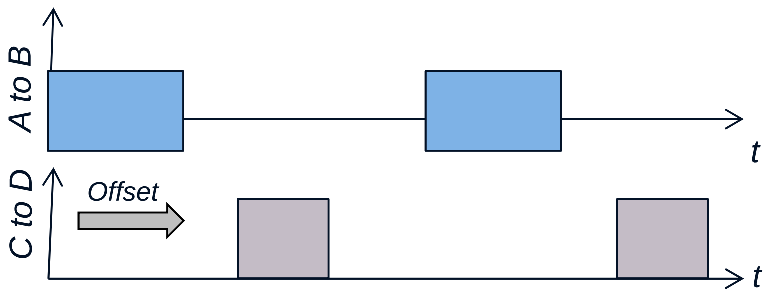
Partitions
Budget
Describe
Resource budget
Architecture
Budgeting
Allocate
Exec. model
Mastering execution
HW config.
Hypervisor
Compile
Executable

Mastering execution

Rule 1: In a compute cluster, each local SRAM bank and each core can be used by at most one partition



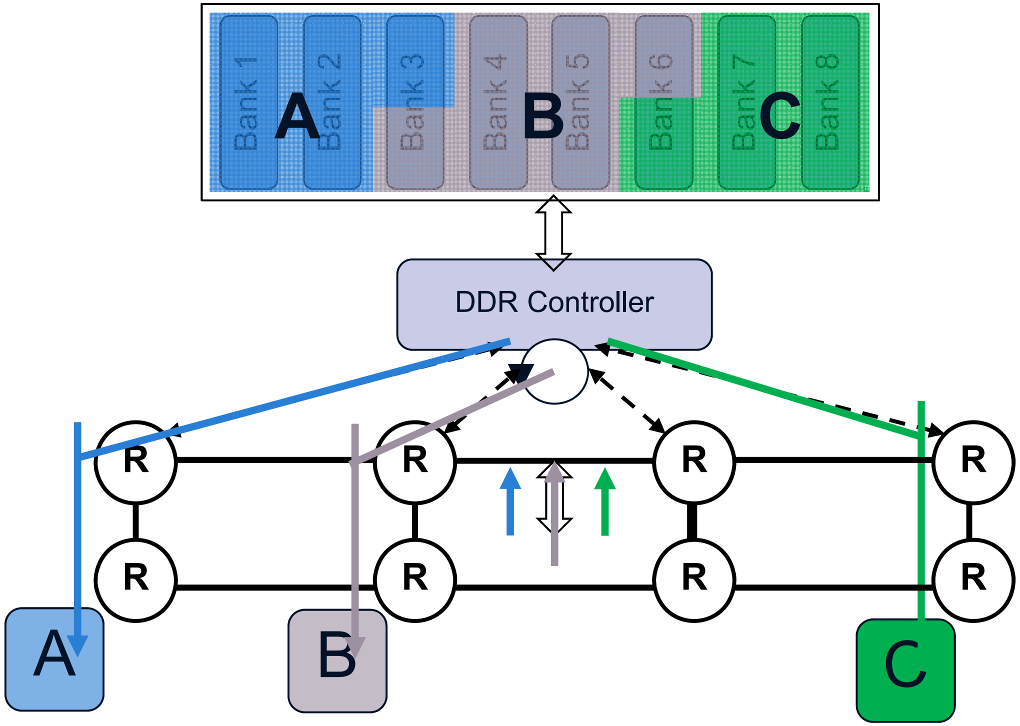
Rule 2: NoC transactions are performed during strictly periodic slots defined off-line and do not overlap (TDMA)

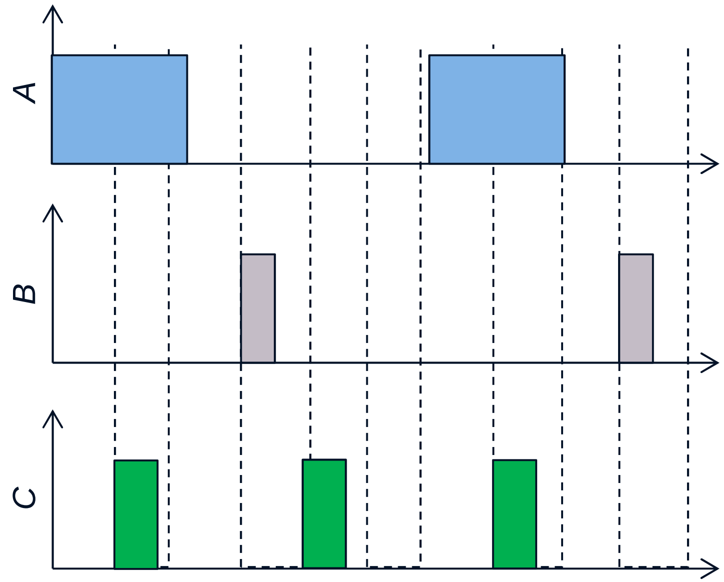


Mastering execution

Rule 3: All the buffers sent during the strictly periodic NoC slots must be defined off-line.

Rule 4: A bank of the DDR-SDRAM can be used by several partitions if and only if they never access it simultaneously.





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Budgeting: Architecture description

Partition Node (or PN): processing resources

- Number of PEs
- Number of SRAM banks

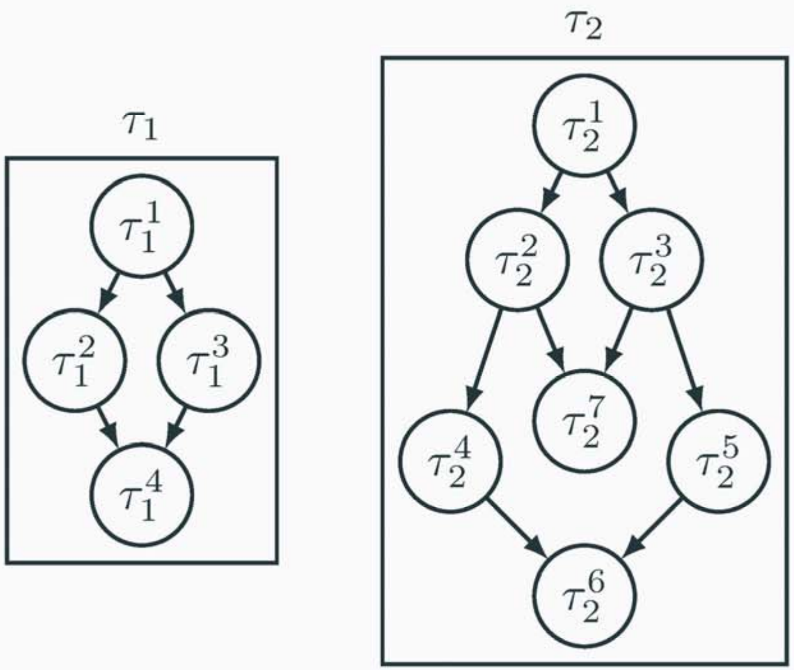
I/O Node (or ION): I/O transactions

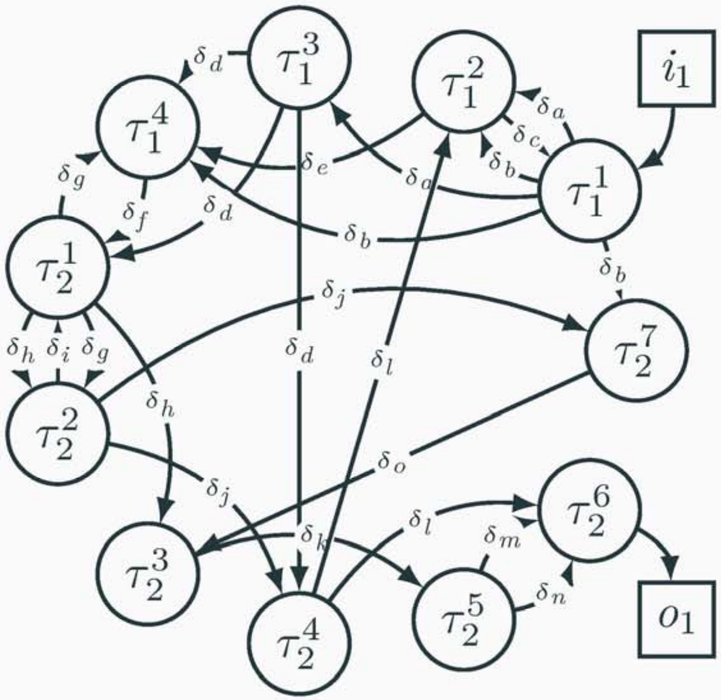
- Core on I/O cluster

Partition Communication (or PC):

- communications between PN / ION
- Source and destination PN / ION
- Period, duration and offset of strictly periodic slot

Budgeting: Application's budget





$$\tau_i =< S_i, P_i, T_i >$$

$$\tau_i^j =< C_i^j, M_i^j, I_i^j, O_i^j >$$

$$\delta_k =< m_k, prod, cons >$$

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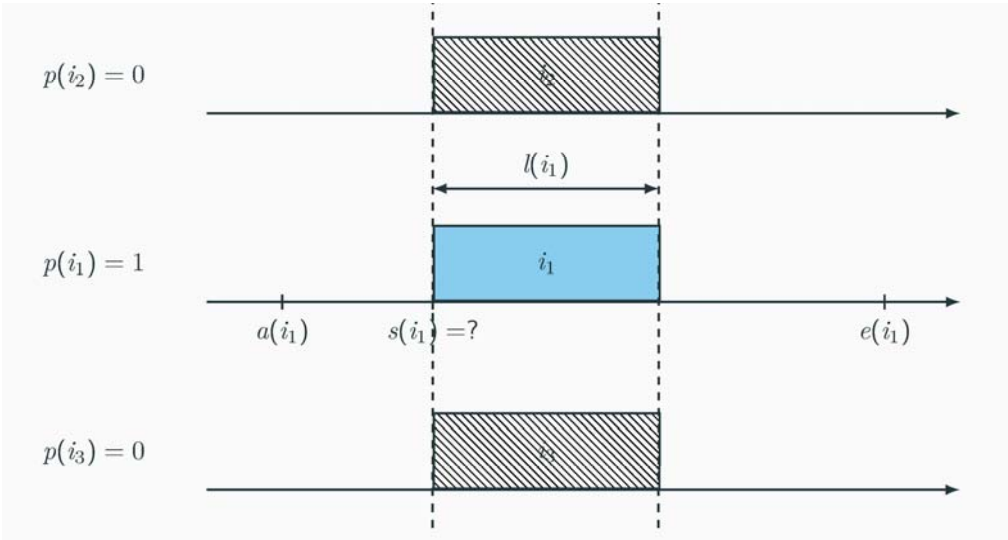
Budgeting: Conditional time-intervals

OPL IBM constraint programming modelling with Conditional Time-Intervals

- Very efficient for non preemptive task

A task t_1 is associated with:

- an interval i_1 of length t.wcet
- n conditional intervals $i_{1,1}$, $i_{1,2}$ …, $i_{1,n}$

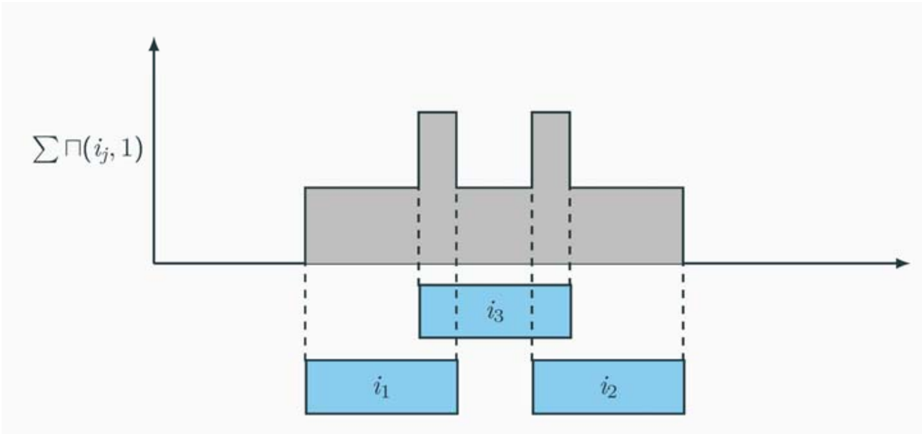


Only 1 interval present in the solution: *alternative*(i_1, *all*($x \in 1,..,n$)$i_{1,x}$)

Solver produces *presenceOf*(i_1,x) and *startOf*(i_1).

Conditional time-intervals

To express that two tasks must not overlap on a core, notion of cumulative function



constraint ***for all core k, Σ pulse*****($i_{x,k}$, 1) ≤ 1**

replace

for all pair of tasks, $c_1 = c_2 \Rightarrow (s_1 + t_1.wcet \leq s_2) \vee (s_2 + t_2.wcet \leq s_1)$

Experimental results

1 PE per PN

- Limit interference at SRAM level
- Focus on NoC-level parallelization

Symmetric PCs

- Each PN can send data to all PNs
- All PCs with same period and duration
- PC duration close to Hypervisor's WCET

Avionic application has been successfully mapped

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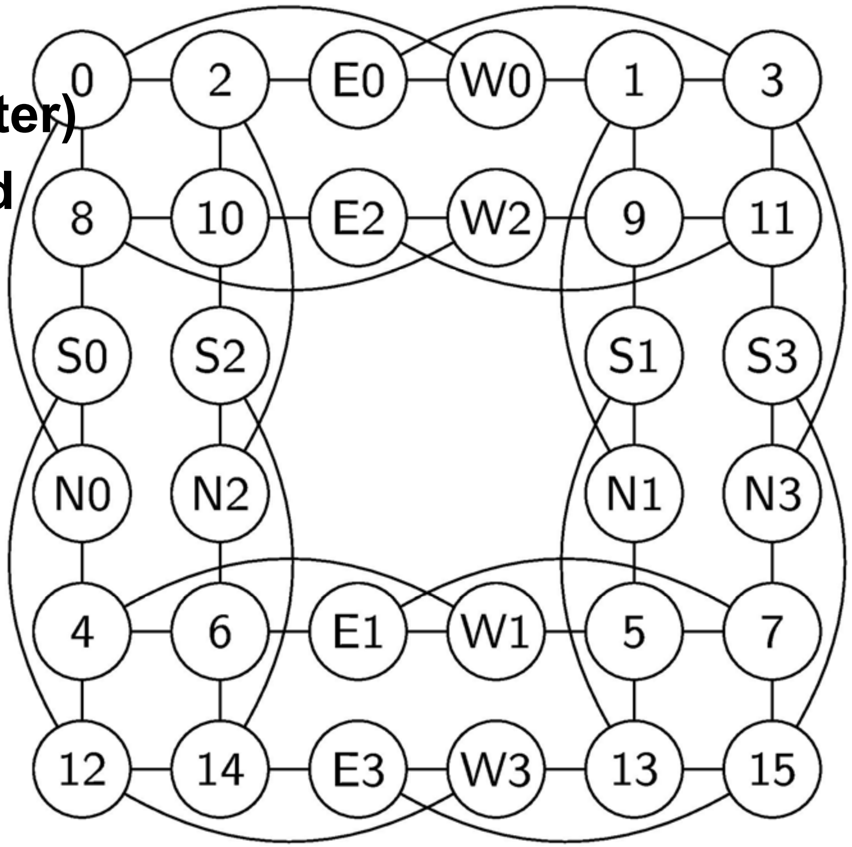
Bounding MPPA network-on-chip traversal time: a network calculus approach

<u>Contributors:</u> **Marc Boyer, Amaury Graillat, Benoît Dupont de Dinechin, Jörn Migge**

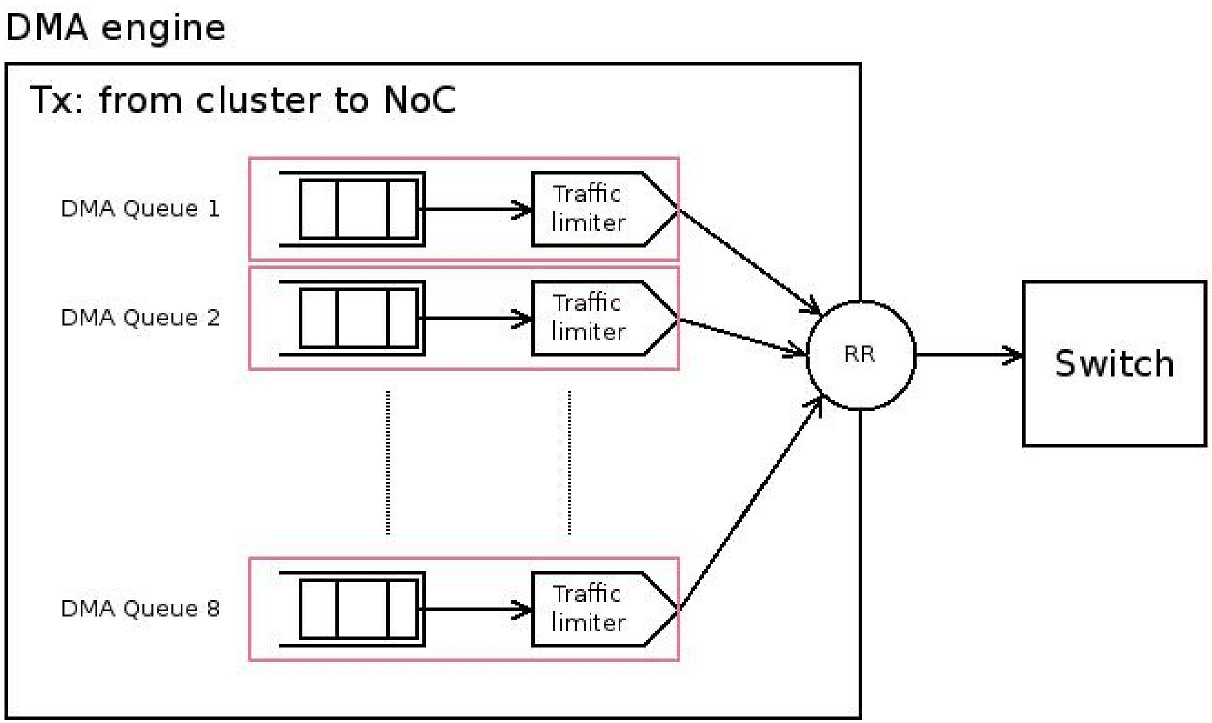
- **16 switches (1 per compute cluster)**
- **16 switches (dedicated to I/O and memory)**
- **connected by a network-on-chip (NoC)**



Computing Routes and Delay Bounds for the Network-on-Chip of the Kalray MPPA2 Processor Marc Boyer, Benoît Dupont de Dinechin, Amaury Graillat, Lionel Havet ERTS 2018

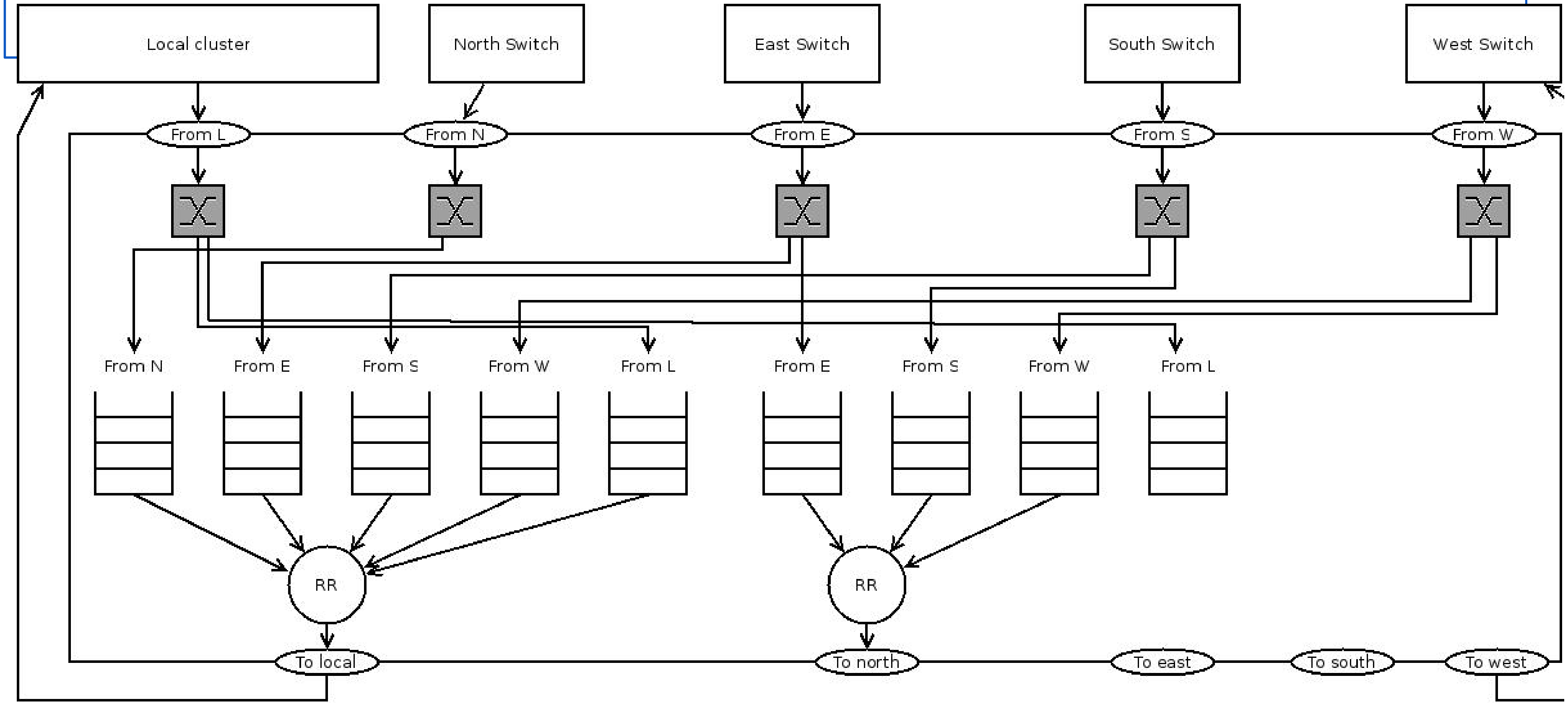
DMA Engine

- **8 queues**
- **a traffic limiter per queue**
  - token-bucket
  - send only full packet
- **Round-Robin arbiter**



Switch

- 5 input ports: East, West, North, South, Local
- 5 output ports
- each output port has one queue per input port
- round-robin arbiter



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A real-time network

- **Traffic limiter + “enough” memory + guaranteed throughput**

  ➔ bounded latency
- **Remarks: MPPA NoC apply “wormhole switching”**
  - when a queue is full, previous switch must stop emission
  - ... then its own queue fills up
  - known as “back pressure”
    - complex analysis
    - can lead to deadlock

  ⇒ limit traffic to never fill queues

- **Challenge: computing a latency bound**
- **Method: network calculus**

https://en.wikipedia.org/wiki/Wormhole_switching

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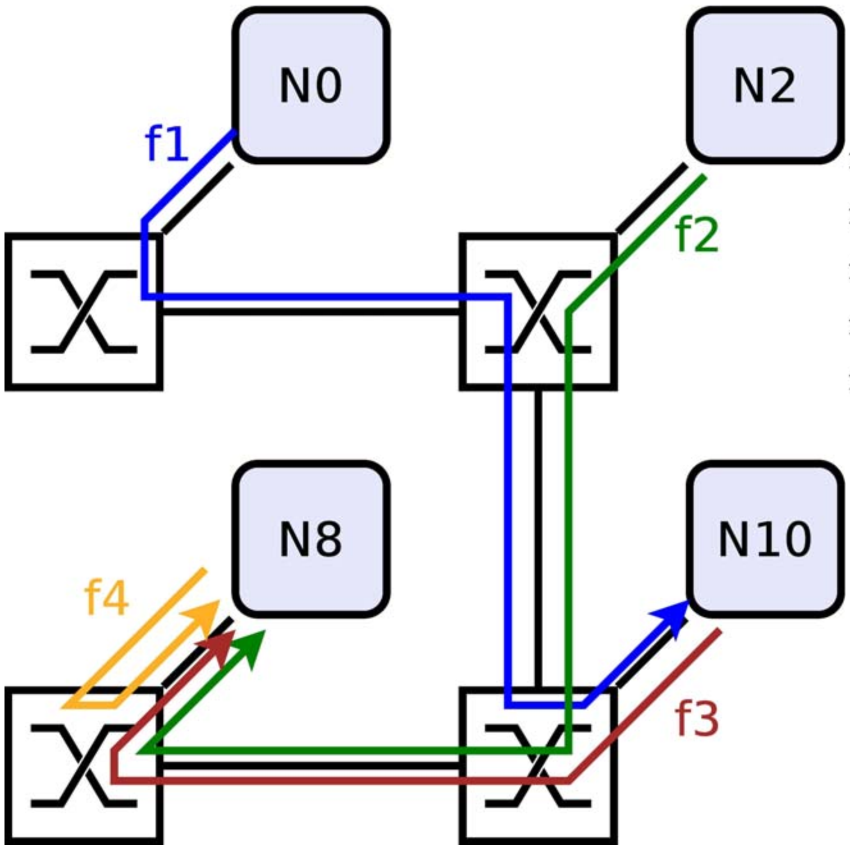
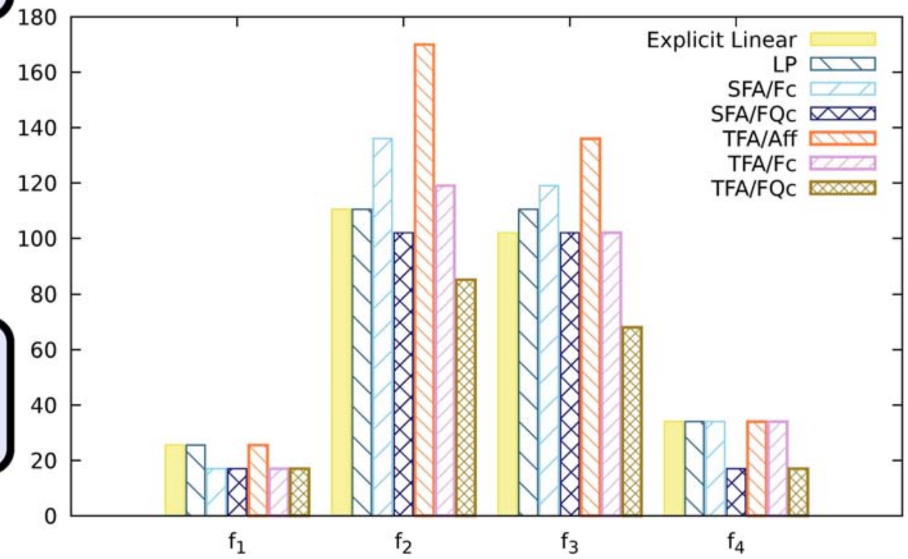
Network calculus: a toolbox

Several approaches used:

- **Explicit Linear: closes expression formula**
- **LP: use of MILP solver**
- **Separated Flow Analysis (SFA): end-to-end network calculus**
- **Total Flow Analysis (TFA): per switch network calculus**

First case study





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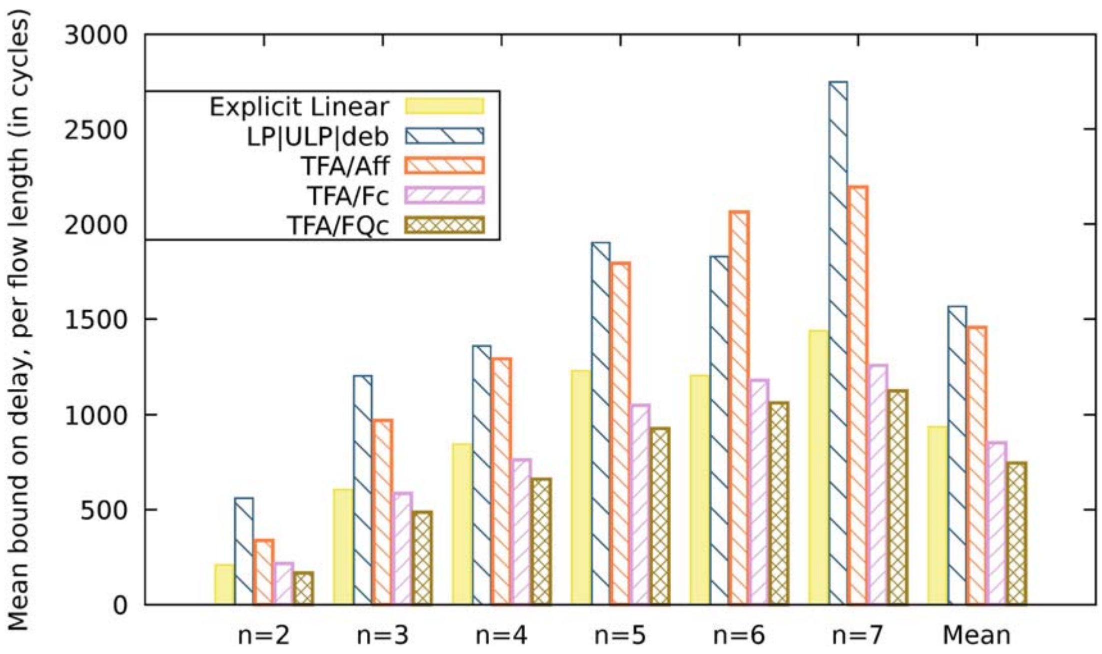
Second case study

- **4 flows out of each switch local port**

  ⇒ 128 flows
- **Random destination (unicast)**
- **figure: average latency bound (grouped per flow length)**



Conclusion on the NoC

- **MPPA NoC supports real-time guaranties**
- **Network calculus permits to compute latency bounds**
- **Delay bounds: ≈ 1µs on large case study**

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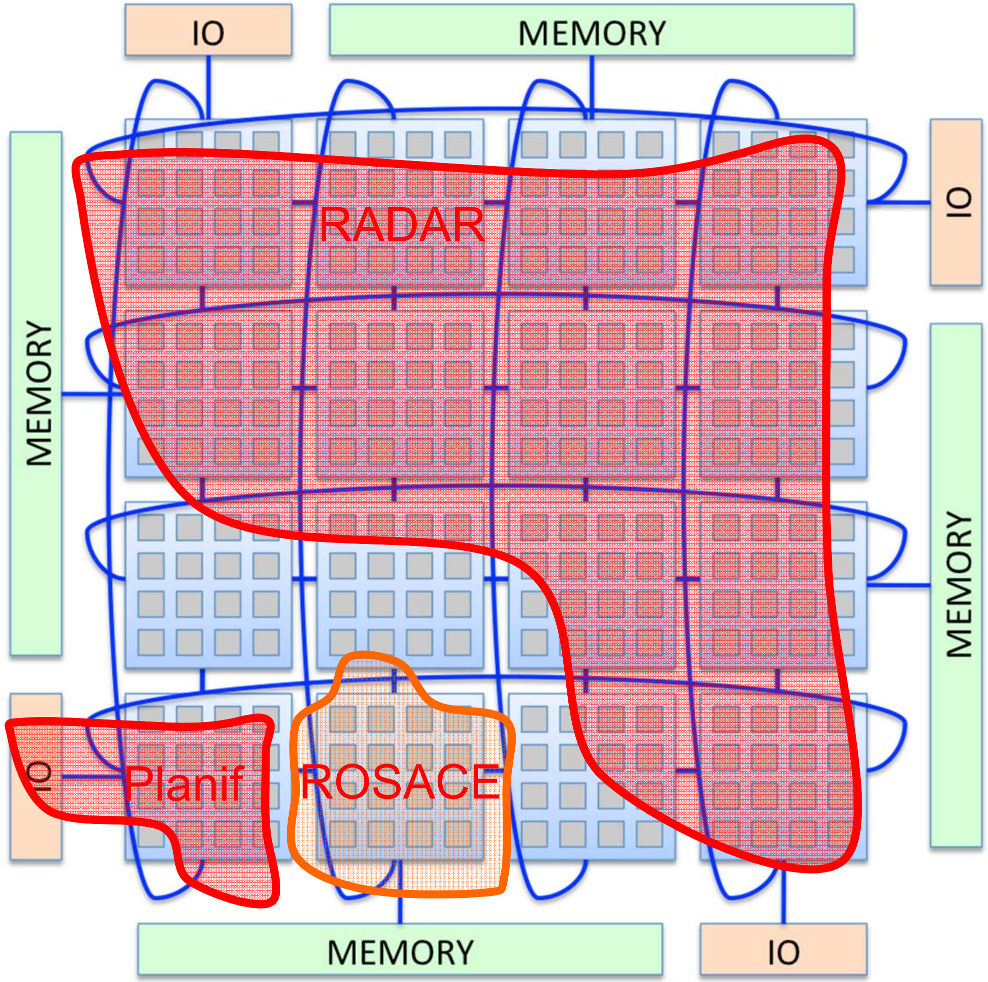
Porting of applications on the MPPA

Contributors: Youcef Bouchebaba, Jean-Loup Farges



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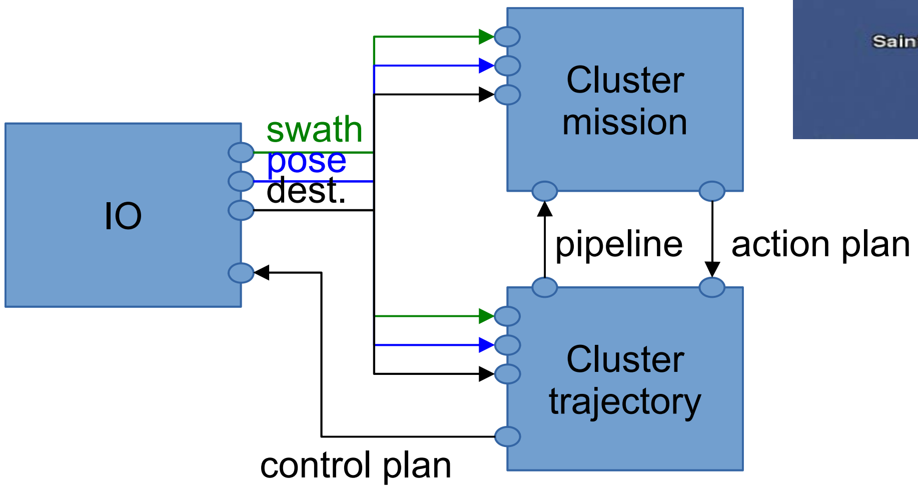
Planning application

1 or 2 clusters involved



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Future work

Coolidge (CAVIAR project 2021 – 2022)

- **WCTT with network calculus**
- **Interference calculus (cf PHYLOG / MCP CRI / CAST 32A)**
- **Safety analysis**